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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,989	12/20/2000	Jeffrey Somers	SRT-009 (5049/15)	7378

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EXAMINER	
PATEL, NIKETA I	
ART UNIT	**PAPER NUMBER**
2182	6

DATE MAILED: 06/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

01

Office Action Summary	Application No.	Applicant(s)	
	09/742,989	SOMERS ET AL.	
	Examiner	Art Unit	
	Niketa I. Patel	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. The term "***substantially***" in **claim 5**, line 2; **claim 2**, line 2; **claim 10**, line 2; **claim 11**, line 2; **claim 16**, line 1; **claim 19**, lines 9, 11; and **claim 22**, line 2 is a relative term which renders the claim indefinite. The term "***substantially***" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an

international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-20 and 22-23 rejected under 35 U.S.C. 102(e) as being anticipated by Barry et al. U.S. Patent Number: 6,457,073 (hereinafter referred to as "*Barry*".)

5. **Referring to claim 1**, *Barry* teaches a method for transferring portions of a memory block comprising the steps of: (a) configuring a first data mover with a first start address corresponding to a first portion of a source memory block (see column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; figure 3 – elements 303, 302); (b) configuring a second data mover with a second start address corresponding to a second portion of the source memory block sized differently from the first portion (see column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; figure 3 – elements 303, 302); (c) transferring, by the first data mover, the first portion of the source memory block (see column 6 – lines 10-67; column 7 – lines 1-31; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-9); and (d) transferring, by the second data mover, the second portion of the source memory block (see column 6 – lines 10-67; column 7 – lines 1-31; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-9.)

6. **Referring to claim 2**, *Barry* teaches to configure the first data mover with a first chunk end address corresponding to the first portion of the source memory block (see column 10 – lines 16-67.)

7. **Referring to claim 3**, *Barry* teaches to generate the first chunk end address (see column 10 – lines 16-67.)

8. **Referring to claim 4**, *Barry* teaches to configure the first data mover with a first write address corresponding to a first portion of a first target memory block (see column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

9. **Referring to claim 5**, *Barry* teaches to transfer of the first portion of the source memory block further comprises stopping when the first start address is *substantially* equivalent to the first chunk end address (see column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

10. **Referring to claim 6**, *Barry* teaches to transfer of the first portion of the source memory block further comprises stopping when the first start address is *substantially* equivalent to a predefined end address (see column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

11. **Referring to claim 7**, *Barry* teaches to configure the second data mover with a second chunk end address (see column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

12. **Referring to claim 8**, *Barry* teaches to generate the second chunk end address (see column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

13. **Referring to claim 9**, *Barry* teaches to configure the second data mover with a second write address corresponding to a second portion of a second target memory block (see column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

14. **Referring to claim 10**, *Barry* teaches to transfer of the second portion of the source memory block further comprises stopping when the second start address is *substantially*

equivalent to the second chunk end address (see column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

15. **Referring to claim 11**, *Barry* teaches to transfer of the second portion of the source memory block further comprises stopping when the second start address is *substantially* equivalent to a predefined end address (see column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

16. **Referring to claim 12**, *Barry* teaches to configure the first data mover as a master data mover and the second data mover as a salve data mover (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

17. **Referring to claim 13**, *Barry* teaches to communicate, by the master data mover, the first start addresses to the slave data mover (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

18. **Referring to claim 14**, *Barry* teaches to transfer the first portion of the source memory block to the first write address corresponding to the first portion of the first target memory block (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

19. **Referring to claim 15**, *Barry* teaches to transfer the second portion of the source memory block to the second write address corresponding to the second portion of the second target memory block (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

20. **Referring to claim 16**, *Barry* comprise *substantially* simultaneously transferring the first portion and the second portion of the source memory block (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67.)

21. **Referring to claim 17**, *Barry* teaches a method for transferring portions of a memory block comprising the steps of: (a) designating a master data mover (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); (b) designating a slave data mover in communication with the master data mover (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); (c) transmitting a start address to the master data mover, the start address identifying a first memory portion of a source memory block (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); (d) transmitting the start address to the slave data mover to enable the slave data mover to determine a next address, the next address identifying a second memory portion of the source memory block sized differently from the first memory portion (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); (e) transmitting a first write address identifying a first memory portion of a target memory block to the master data mover and a second write address identifying a second memory portion sized differently then the first memory portion of the target memory block to the slave data mover (see column 18 – lines 4-67; column 19 – lines

1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); (f) copying the first memory portion of the source memory block to the first write address identifying the first memory portion of the target memory block (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); and (g) transferring the second memory portion of the source memory block to the second write address identifying the second memory portion of the target memory block (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302.)

22. **Referring to claim 18**, *Barry* teaches to verify that the master data mover is available; (i) transmitting a first end address associated with the first memory portion of the source memory block to the master data mover and a second end address associated with the second memory portion to the slave data mover (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); and (j) synchronizing the master data mover with the slave data mover (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302.)

23. **Referring to claim 19**, *Barry* teaches (h) transmit a first offset address to the master data mover and a second offset address to the master data mover (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); (i) obtaining, by the master data mover, a first next address by using the first offset address and the start address (see column 18 – lines

4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); (j) obtaining, by the slave data mover, a second next address by using the second offset address and the start address (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); (k) stopping the transmitting of the first memory portion of the source memory block after the first next address is *substantially* equivalent to the first end address (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); and (l) stopping the transmitting of the second memory portion of the source memory block after the second next address is *substantially* equivalent to the second end address (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302.)

24. **Referring to claim 20**, *Barry* teaches a system to transfer portions of a memory block comprising: (a) a first data mover (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); (b) a second data mover in communication with the first data mover over a DM communications bus (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); (c) a first memory component having a first portion and a second portion sized differently from the first portion and in communication with the first data mover and the second data mover over a first DM-memory bus (see column 18 – lines 4-67;

column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302); and a second memory component in communication with the first data mover and the second data mover over a second DM-memory bus, wherein the first data mover transfers the first memory portion to the second memory component over the first DM-memory bus at a first data transfer rate, and wherein the second data mover transfers the second memory portion to the second memory component over the second DM-memory bus at a second data transfer rate (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302.)

25. **Referring to claim 22,** *Barry* teaches that the first data mover transfers the first memory portion at a *substantially* simultaneous time as the second data mover transfers the second memory portion (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302.)

26. **Referring to claim 23**, *Barry* teaches that the first data mover is a first Direct Memory Access (DMA) engine and the second data mover is a second DMA engine (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302.)

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barry et al. U.S. Patent Number: 6,457,073 (hereinafter referred to as "*Barry*".) as applied to claim 20 above, and further in view of Priem et al. U.S. Patent Number: 6,065,071 (hereinafter referred to as "*Priem*".)

29. **Referring to claim 21**, *Barry* teaches a first DM-memory bus and a second DM-memory bus (see column 18 – lines 4-67; column 19 – lines 1-41; column 2 – lines 14-32; column 5 – lines 1-28, 48-67; column 6 – lines 1-37; column 10 – lines 16-67; figure 3 – elements 303, 302.) *Barry* fails to explicitly set forth the limitation that the first DM-memory bus is a Peripheral Component Interconnect (PCI) bus and the second DM-memory bus is an Accelerated Graphics Port (AGP) bus. However, *Priem* teaches a use of PCI bus and an AGP bus (see column 4 – lines 30-42) to accomplish faster transfers of data directly from an application program to I/O devices (see column 2 – lines 34-62.)

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the first DM-memory bus and the second DM-memory bus of *Barry* to be a PCI bus and an AGP bus to accomplish faster transfers of data directly from an application program to I/O devices. It is for this reason that one of ordinary skill

in the art would have been motivated to substitute *Barry's* first and second DM-memory buses with a PCI bus and an AGP bus to allow for a direct data transfer from an application program to I/O devices.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents have been made record of to further show the state of the art as it pertains to direct memory access controllers.

Amrany et al. U.S. Patent Number: 6,412,027

Habot U.S. Patent Number: 6,453,365

Seshan et al. U.S. Patent Number: 6,145,027

Kubo U.S. Patent Number: 6,557,052

Pham et al. U.S. Patent Number: 6,493,803

West U.S. Patent Number: 6,195,730

Yanagisawa et al. U.S. Patent Number: 6,209,042

Schultz U.S. Patent Number: 6,012,109

Goh et al. U.S. Patent Number: 6,373,841

Nagaraj et al. U.S. Patent Number: 5,805,842

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (703) 305 4893. The examiner can normally be reached on M-F 9:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (703) 308 3301. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746 7239 for regular communications and (703) 746 7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305 3900.

NP
June 25, 2003

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100